What is claimed is:

1. A semiconductor device comprising:

external contacts;

a metal layer; and

a passivation layer being located between the metal layer and the contact and including windows through which the contacts extend to make electrical connections with the metal layer, the windows being selectively size to impart a higher current carrying capability to at least one of the external contacts than to the remaining one or more external contacts.

2. The semiconductor device of claim 1, wherein the external contacts comprise solder bumps.

3. The semiconductor device of claim 1, further comprising:

a power bus in communication with at least one of the external contacts that have a higher current carrying capability.

4. The semiconductor device of claim 1, wherein at least one of the external contacts that have a higher current carrying capability is elongated along an axis that generally follows a bus to which the external contact is connected.

5. The semiconductor device of claim 1, wherein the metal layer comprises a conductive region in contact with the solder bump, the region being elongated along another axis that is generally aligned with said at least part of the path.

6. The semiconductor device of claim 1, wherein the path comprises an approximately straight line and the axis is generally parallel to the straight line.

7. The semiconductor device of claim 1, wherein at least one of the windows comprises one of a rectangular window and a hexagonal window.

8. The semiconductor device of claim 1, wherein the windows comprise a first set of at least one window that has a first size and a second set of at least one window that has a significantly larger second size.

9. An electrical device comprising:

electrical contact pads to receive a supply voltage;

a power bus electrically connected to the electrical contact pads; and

an interconnection circuit to, for each electrical contact pad, form a redundant connection between the bus and the electrical contact pad.

10. The electrical device of claim 9, wherein

the electrical device comprises a semiconductor device comprising having multiple process layers, and

the interconnection circuit is formed in the same process layer as the power bus.

11. The electrical device of claim 9, wherein

the electrical device comprises a semiconductor device comprising having multiple process layers, and

the interconnection circuit is formed in one of the process layers located between another one of the process layers in which the bus is formed and the electrical contacts.

12. The electrical device of claim 9, wherein the interconnection circuit comprises:

switches to selectively form the redundant connections.

13. The electrical device of claim 9, wherein the device comprises a microprocessor.

14. A method usable with a semiconductor device, comprising:

providing a passivation layer;

providing windows in the passivation layer;

extending external contacts through the window to make an electrical connection with a metal layer of the semiconductor device; and

selectively sizing the windows to impart a higher current capability to at least one of the external contacts than to the remaining one or more external contacts.

15. The method of claim 14, wherein the external contacts comprise solder bumps.

16. The method of claim 14, further comprising:

providing a power bus in communication with at least one of the external contacts that have a higher current carrying capability.

17. The method of claim 14, wherein the path comprises an approximately straight line and the axis is generally parallel to the straight line.

18. The method of claim 14, wherein at least one of the windows comprises one of a rectangular and a hexagonal window.

19. The method of claim 14, wherein the windows comprise a first set of at least one window that has a first size and a second set of at least one window that has a significantly larger second size.

20. A method usable with a semiconductor device, comprising:

electrical connecting external contacts of a semiconductor device to internal buses of the semiconductor device; and

establishing redundant connections between the buses and the external contacts.

21. The method of claim 20, further comprising:

forming the buses in a first process layer; and

forming the redundant connections in the same first process layer.

22. The method of claim 20, further comprising:

forming the buses in a first process layer; and

forming the redundant connections in a second process layer different from the first process layer.

23. The method of claim 20, further comprising:

forming a passivation layer;

providing contacts that are exposed for external connections with the semiconductor device on one side of the passivation layer; and

forming the redundant connections on said one side.

24. The method of claim 23, wherein the forming comprises:

depositing a metal layer on said one side; and

selectively etching the metal layer to form the redundant connections.